REMARKS

This amendment is responsive to the Office Action dated July 22, 2005. Applicant has amended claims 39, 41, 43, 44, 52 and 56. Claims 39-73 are pending.

Claim Objection

In the Office Action, the Examiner objected to claims 39, 41, 43, 44, and 52 for use of the phrase "adapted to". The Examiner asserted that use of this phrase is optional language according to MPEP 2106.II.C. Applicants have amended claims 39, 41, 43, 44, 52 and 56 to remove the phrase "adapted to" as requested by the Examiner. Applicants request withdrawal of the objection.

Claim Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 39-44 and 46-73 under 35 U.S.C. 102(e) as being anticipated by Dai et al. (USPN 6,658,016). Applicant respectfully traverses the rejection. Dai et al. (Dai) fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

Dai fails to teach or suggest an apparatus having a set of data rings in communication with said set of input ports and said set of sink ports, wherein at least one of the sink ports in said set of sink ports *concurrently* receives a plurality of data packets from two or more of the data rings, as recited by Applicants' independent claim 39 as amended.

Regarding claim 39, the Examiner asserted that Dai teaches a set of input ports (88), a set of sink ports (84), and a set of data rings (16, 22) in communication with the set of input ports (88) and the set of sink ports (84). The Examiner also stated that the Dai reference teaches each sink port in the set of sink ports *concurrently* receiving a plurality of data packets by simultaneously transmitting the data stream to the network output ports. The Examiner referred to Col. 8, ll. 50-61 of Dai for support of the rejection. However, the cited passage merely teaches that while a data stream is received at the data ring input 16 of the device 12 from an upstream source device, preceding data of the same data stream is simultaneously transmitted from the appropriate one of network output ports 84. Thus, Dai is referring to simultaneous forwarding

and transmission of a single data stream. Dai is describing forwarding a packet of a data stream while receiving a different (subsequent) packet of that data stream. Dai makes no mention of an output port 84 receiving a *plurality* of data packets concurrently, i.e., *at the same time, from different data rings*. The Dai reference fails to teach each of the output (sink) ports *concurrently* receiving data packets at all, let alone from different data rings.

Moreover, Dai fails to describe *an apparatus* (e.g., a crossbar switch) having a set of data rings in communication with the set of input ports and the set of sink ports *within that same apparatus*. Instead, Dai describes a packet switching fabric in which a plurality of switching devices are coupled in a ring fashion. The Dai switch fabric is properly viewed as a ring of switches. For example, FIG. 1 of Dai illustrates four distinct switching devices 12 coupled in a ring-like manner using an external data ring 18 and a control ring 24. The data ring 18 includes a plurality of data ring segments each coupling a corresponding adjacent pair of the devices together to ultimately form a ring.

In the Dai switch fabric, packets may propagate from switch to switch and ultimately may traverse the ring of switches. As can be seen by FIG. 1, to traverse the ring, a packet must be sequentially propagated by each of the switches. Each of switches 12 in the ring is a separate switch having input and output (sink) ports, and further includes ring interface circuitry so that the switches may be interconnected to form an overall ring of switches.

In contrast, Applicants describe and claim a *single* apparatus, e.g., a cross-bar switch, in which the apparatus itself includes data rings for transferring packets directly between the input ports and the output (sink) ports of that same apparatus. For purposes of clarity, Applicants refer the Examiner to Figure 2 of the present application that illustrates exemplary internal architecture of Applicants' described apparatus. When properly viewed, the Dai switches that may be connected to form a "ring" are fundamentally different from the internal apparatus architecture described and claimed by the Applicants. Dai fails to teach or suggest that the internal architecture of any of the switches comprises a ring topology that connects the input ports and the output ports within the individual switch. Thus, the Examiner is incorrect when asserting that Dai teaches an apparatus comprising a set of input ports to receive data packets, a set of sink ports in communication with said set of input ports to receive and forward said data packets, and a set of data rings in communication with said set of input ports and said set of sink ports.

Dai also fails to teach or suggest a set of input ports to receive data packets, and a set of sink ports in communication with said set of input ports to receive and forward said data packets, wherein said first sink port receives a first data packet and a second data packet, and said first sink port receives a portion of said second data packet at a time when said first sink port receives said first data packet, as recited by Applicants' independent claim 52.

In support of the rejection of claim 52, the Examiner asserted that Dai teaches the first sink port receiving a portion of the second data packet at a time when the first sink port receives said first data packet by one of the output ports 84 receiving the first one or two bursts of data packets in a pipelined manner. The Examiner referred to Col. 21, ll. 20-65 of the Dai reference, which describes determining available space in a transmit buffer 80 of each of the output (sink) ports 84 sufficient for accommodating one or two data bursts. The cited passages further state that the first one or two data bursts may be transferred from the source device to the destination device in a pipeline manner.

Applicants submit that the Examiner has misinterpreted the scope of the Dai reference. Dai fails to teach an output (sink) port that receives a second data packet at approximately the same time as the output port receives a first data packet. Instead, Dai merely describes receiving sequential data packets in a transmit buffer of an output port. Dai teaches determining a number of data bursts that may be temporarily stored in the transmit buffer so as not to overload the transmit buffer. Dai never mentions receiving more than one of the data bursts at the same time. Furthermore, transmitting the data bursts in a pipelined manner clearly refers to a sequential transmission of the data bursts in which a second data burst is transmitted directly after a first data burst, as if flowing through a pipeline. Dai fails to disclose or suggest an output port receiving at least a portion of a second data packet during the time when the output port is receiving a first data packet.

With respect to Applicants' independent claim 60, Dai fails to teach or suggest receiving a set of data packets, transferring said set of data packets to a set of data rings in communication with a set of sink ports, and a sink port in said set of sink ports collecting data for data packets accepted by said sink port, wherein collecting data includes the steps of: said sink port collecting data for a first data packet, and said sink port collecting data for a portion of a second data packet during a time period when said sink port is collecting data for the first data packet.

Regarding claim 60, the Examiner asserted that Dai teaches transferring a set of data packets to a set of data rings in communication with a set of sink ports. However, Dai fails to describe *an apparatus* having a set of data rings in communication with the set of sink ports *within the apparatus*. Instead, Dai describes a packet switching fabric in which a plurality of switching devices are coupled in a ring fashion. As described above, the Dai switch fabric is properly viewed as a ring of switches. For example, FIG. 1 of Dai illustrates four distinct switching devices 12 coupled in a ring-like manner using an external data ring 18 and a control ring 24. The data ring 18 includes a plurality of data ring segments each coupling a corresponding adjacent pair of the devices together to ultimately form a ring.

In contrast, Applicants describe and claim a single apparatus, e.g., a cross-bar switch, in which the apparatus itself includes data rings for transferring packets directly between the input ports and the output (sink) ports of that same apparatus. For purposes of clarity, Applicants refer the Examiner to Figure 2 of the present application that illustrates exemplary internal architecture of Applicants' described apparatus. When properly viewed, the Dai switches that may be connected to form a "ring" are fundamentally different from the internal apparatus architecture described and claimed by the Applicants. Dai fails to teach or suggest that the internal architecture of any of the switches comprises a ring topology that connects the input ports and the output ports within the individual switch. Thus, the Examiner is incorrect when asserting that Dai teaches transferring a set of data packets to a set of data rings in communication with a set of sink ports.

Furthermore, the Examiner stated that the Dai reference teaches the sink port collecting data for a first data packet, and the sink port collecting data for a portion of a second data packet during a time period when the sink port is collecting data for the first data packet. The Examiner again referred to Col. 21, ll. 20-65 of the Dai reference, which describes determining available space in a transmit buffer 80 of each of the output (sink) ports 84 sufficient for accommodating one or two data bursts. The cited passages further state that the first one or two data bursts may be transferred from the source device to the destination device in a pipeline manner.

As described above, Dai fails to teach an output (sink) port that collects data for a second data packet at approximately the same time as the output port collects data for a first data packet. Instead, Dai merely describes receiving sequential data packets in a transmit buffer of an output

port. Dai teaches determining a number of data bursts that may be temporarily stored in the transmit buffer so as not to overload the transmit buffer; Dai never mentions collecting data for more than one of the data bursts at the same time. Furthermore, transmitting the data bursts in a pipelined manner clearly refers to a sequential transmission of the data bursts in which a second data burst is transmitted directly after a first data burst, as if flowing through a pipeline. Dai fails to disclose or suggest an output port collecting data for at least a portion of a second data packet during the time when the output port is collecting data for a first data packet.

Regarding Applicants' independent claim 67, Dai fails to teach or suggest a method comprising the steps of receiving a set of data packets on a set of input ports, wherein receiving the set of data packets includes the steps of receiving a first data packet and receiving a second data packet, a sink port in a set of sink ports in communication with said set of input ports, collecting data for data packets accepted by said sink port, wherein collecting data includes the steps of said sink port collecting data for said first data packet, and said sink port collecting data for a portion of said second data packet during a time period when said sink port is collecting data for said first data packet.

In support of the rejection of claim 67, the Examiner stated that the Dai reference teaches the sink port collecting data for a first data packet, and the sink port collecting data for a portion of a second data packet during a time period when the sink port is collecting data for the first data packet. The Examiner again referred to Col. 21, ll. 20-65 of the Dai reference, which describes determining available space in a transmit buffer 80 of each of the output (sink) ports 84 sufficient for accommodating one or two data bursts. The cited passages further state that the first one or two data bursts may be transferred from the source device to the destination device in a pipeline manner.

As described above, Dai fails to teach an output (sink) port that collects data for a second data packet at approximately the same time as the output port collects data for a first data packet. Instead, Dai merely describes receiving sequential data packets in a transmit buffer of an output port. Dai teaches determining a number of data bursts that may be temporarily stored in the transmit buffer so as not to overload the transmit buffer; Dai never mentions collecting data for more than one of the data bursts at the same time. Furthermore, transmitting the data bursts in a pipelined manner clearly refers to a sequential transmission of the data bursts in which a second

data burst is transmitted directly after a first data burst, as if flowing through a pipeline. Dai fails to disclose or suggest an output port collecting data for at least a portion of a second data packet during the time when the output port is collecting data for a first data packet.

Dai similarly fails to disclose the features required by Applicants' dependent claims 40-51, 53-59, 61-66 and 68-73. For example, claim 40 recites each data packet in said plurality of data packets having a same destination address. In support of the rejection, the Examiner asserted that Dai teaches a data stream which is a collection of data packets transmitted to an appropriate one of the network output ports. Dai makes no mention of each of the data packets having the same destination address. Instead, Dai describes the output ports receiving a continuous stream of packets from the data ring input of the switch such that different data packets of the same stream of packets are simultaneously received at the data ring input and the appropriate output port. The Dai reference fails to teach each of the data packets having the same destination address.

In addition, claims 53, 61 and 68 recite that the first data packet is targeted to a first destination and said second data packet is targeted to said first destination. The Examiner asserted that determining that two blocks of space are available in a transmit buffer for accommodating two bursts of data packets anticipates this feature. As discussed above, Dai teaches determining a number of data bursts that may be temporarily stored in the transmit buffer so as not to overload the transmit buffer. Dai never mentions a first data packet and a second data packet received by a single output port at approximately the same time being targeted to the same destination.

As another example, Applicants' claims 42 and 57 recite that said set of data rings couples each sink port in said set of sink ports to each input port in said set of input ports. In support of the rejection, the Examiner cited FIG. 2A of Dai as illustrating that the set of data rings (16, 22) couples each sink port (84) to each input port (88). However, the data rings illustrated in FIG. 2A couple a data ring processing circuit (66) within the switching device to other switching devices. As discussed above, Dai does not teach the data ring coupling each sink port to each input port within the individual apparatus, but instead teach a data ring coupling separate apparatuses together.

Applicants' claims 43 and 54 recite a first sink port in said set of sink ports that receives a first data packet in said plurality of data packets and a second data packet in said plurality of data packets, wherein a first input port in said set of input ports sources said first data packet, and a second input port in said set of input ports sources at least a portion of said second data packet during a time when said first input port sources said first data packet. Dai fails to describe a single output (sink) port receiving first and second data packets sourced from a first input port and a second input port, respectfully, at approximately the same time. The Examiner cited Col. 13, line 1 – Col. 14, line 35 of the Dai reference in support of the rejection, but the cited passages merely discuss components and ports included in a destination management unit of the switching device. Nowhere does Dai mention a single output port capable of receiving two different data packets when the two different data packets were sourced from two different input ports at approximately the same time.

Applicants' claim 62 and 69 recite receiving said first data packet, and receiving a portion of said second data packet during a time period when said first data packet is received. In the Office Action, the Examiner referred to Col. 21, lines 20-65 of the Dai reference and stated that Dai teaches receiving the first one or two bursts of data in a pipelined manner. However, Dai fails to teach receiving a second data packet at approximately the same time as receiving a first data packet. Instead, Dai merely describes receiving sequential data packets in a transmit buffer of an output port. Dai never mentions collecting data for more than one of the data bursts at the same time. Furthermore, transmitting the data bursts in a pipelined manner clearly refers to a sequential transmission of the data bursts in which a second data burst is transmitted directly after a first data burst, as if flowing through a pipeline.

In order to support an anticipation rejection under 35 U.S.C. 102(e), it is well established that a prior art reference must disclose each and every element of a claim. This well known rule of law is commonly referred to as the "all-elements rule."[1] If a prior art reference fails to disclose any element of a claim, then rejection under 35 U.S.C. 102(e) is improper. [2]

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[1] *See Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (CAFC 1986) ("it is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention").
[2] *Id. See also Lewmar Marine, Inc. v. Barient, Inc.* 827 F.2d 744, 3 USPQ2d 1766 (CAFC 1987); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (CAFC 1990); *C.R. Bard, Inc. v. MP Systems, Inc.*, 157 F.3d 1340, 48 USPQ2d 1225 (CAFC 1998); *Oney v. Ratliff*, 182 F.3d 893, 51 USPQ2d 1697 (CAFC 1999); *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 57 USPQ2d 1057 (CAFC 2000).

Dai fails to disclose each and every limitation set forth in claims 39-44 and 46-73. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicant's claims 39-44 and 46-73 under 35 U.S.C. 102(e). Withdrawal of this rejection is requested.

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claim 45 under 35 U.S.C. 103(a) as being unpatentable over Dai in view of Yamamoto et al. (USPN 6,392,991). Applicants respectfully traverse the rejection. The applied references fail to disclose or suggest the invention defined by Applicants' claim, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

Dai and Yamamoto et al. (Yamamoto), either singularly or in combination, fail to describe each and every feature of Applicants' independent claim 39 with said set of data rings including three rings, as recited by Applicants' dependent claim 45. As described above, Dai fails to teach an apparatus having a set of data rings in communication with a set of input ports and a set of sink ports, wherein at least one of the sink ports in the set of sink ports concurrently receives a plurality of data packets from two or more of the data rings. Yamamoto provides no teaching capable of overcoming the deficiencies of Dai.

For at least these reasons, the Examiner has failed to establish a prima facie case for non-patentability of Applicants' claim 45 under 35 U.S.C. 103(a). Withdrawal of this rejection is requested.

Rejection for Obviousness-type Double Patenting:

The Examiner provisionally rejected claim 39 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 09/900,514.

Applicants note the provisional status of this rejection. Accordingly, Applicants will address this issue if and when the rejection is formally applied.

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed agent to discuss this application.

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